6.2 DM1321

6.2.1 General information

The DM1321 module has eight digital channels that can be configured as inputs or outputs. The inputs are designed for sink connections and the outputs for source connections.

- 8 digital channels, can be configured as input or output
- Outputs with short circuit protection
- Outputs with single channel diagnostics
- Configurable input delay
- 2 channels are event counters which also support gate measurement

6.2.2 Order data

Model number	Short description	Figure
	Digital mixed module	
X67DM1321	X67 digital mixed module, 8 channels can be configured as input or output, 24 VDC, 0.5 A, configurable input filter, 2 event counter 50 kHz, LED status indicators	
	Required accessories	
See 14 "Overview of pin connections" on page 647		

Table 172: DM1321 - Order data

6.2.3 Technical data

Product ID	DM1321
Short description	
I/O module	8 digital channels, configured as inputs or outputs using software, inputs with special functions
Rated voltage	24 VDC
Digital inputs	
Input filter Hardware Software	 ≤10 µs (channels 1 - 4) / ≤70 µs (channels 5 - 8) Default 0 ms, can be configured between 0 and 25 ms in 0.2 ms intervals
Input circuit	Sink
Additional functions for inputs	50 kHz event counting, gate measurement
Digital outputs	
Rated output current	0.5 A
Total current	4.0 A
Output circuit	Source
Output protection	Thermal cutoff for overcurrent and short circuit, integrated protection for switching inductances, reverse polarity protection for output supply
General information	
Status indicators	I/O function for each channel, supply voltage, bus function
Diagnostics I/O supply Outputs	 Yes, with status LED and software status Yes, with status LED and software status
Electrical isolation Channel - Bus Channel - Channel	 Yes No
Sensor/actuator supply	0.5 A total current
Power consumption X2X Link supply I/O internal	 0.75 W 2.5 W
Connection type X2X Link Inputs/outputs Module supply	 M12 (B-coded) M8 (3-pin) M8 (4-pin)
Certification Ex zone 2	CE, cRUus, GOST-R, BG tested [1)] II 3G EEx nA II T5, IP67, Ta = 0 - 60°C
Operational conditions	
Operating temperature	0 to +60°C
Mounting orientation	Any
Installation at altitudes above sea level 0 - 2000 m >2000 m	 No derating Reduction of ambient temperature by 0.5°C per 100 m
Protection type	IP67

Table 173: DM1321 - Technical data

Product ID	DM1321
Storage and transport conditions	
Temperature	-25 to +85°C
Mechanical characteristics	
Dimensions (W x H x D)	53 x 85 x 42 mm
Weight	190 g
Torque for connections M8 M12	 Max. 0.4 Nm Max. 0.6 Nm

Table 173: DM1321 - Technical data (Forts.)

1) Operating principle checked: Shutdown initiated by external safety switching device

6.2.4 Additional technical data

Product ID	DM1321
Module supply	
Rated voltage	24 VDC
Voltage range	18 - 30 VDC
Integrated protection	Reverse polarity protection
Power consumption Sensor/actuator supply	 Max. 12 W [1)]
Sensor/actuator supply	
Voltage	Module supply minus voltage drop for short circuit protection
Voltage drop for short circuit protection at 500 mA	Max. 2 VDC
Total current	Max. 0.5 A
Short circuit protection	Yes
Digital inputs	
Input voltage	18 - 30 VDC
Input current at 24 VDC	Typ. 4.0 mA
Input resistance	Typ. 5 kΩ
Switching threshold Low High	 <5 VDC >15 VDC

Table 174: DM1321 - Additional technical data

Product ID	DM1321
Event counter	
Number of counters	2
Counter 1	Input 1
Counter 2	Input 3
Signal form	Square wave pulse
Input frequency	Max. 50 kHz
Counter frequency	Max. 50 kHz
Counter size	16-bit
Evaluation	Each negative edge, cyclic counter
Gate measurement	
Number of gate measurements	1
Gate measurement using	Input 2 or Input 4
Signal form	Square wave pulse
Evaluation	Positive edge - Negative edge
Pulse length	≥20 µs
Length of pauses between pulses	≥100 µs
Internal counter frequency	48 MHz, 3 MHz, 187.5 kHz
Counter size	16-bit
Digital outputs	
Design	FET positive switching
Switching voltage	Module supply minus residual voltage
Diagnostics status	Output monitoring with 10 ms delay
Leakage current when switched off	5.0 µA
Residual voltage	<0.3 V @ 0.5 A rated current
Short circuit peak current	<12.0 A
Switching on after overload cutoff	Approx. 10 ms (depends on the module temperature)
Switching delay $0 \rightarrow 1$ $1 \rightarrow 0$	 <400 µs <400 µs
Switching frequency Resistive load Inductive load	 Max. 100 Hz See the section 6.2.13 "Switching inductive loads" on page 260 (at 90% duty cycle)
Braking voltage when switching off inductive loads	50 VDC
General information	
Isolation voltage betw. channel and bus	500 V_{eff}
B&R ID code	$1311

Table 174: DM1321 - Additional technical data (Forts.)

1) The power consumption of the sensors and actuators connected to the module should not exceed 12 W.

6.2.5 Status LEDs

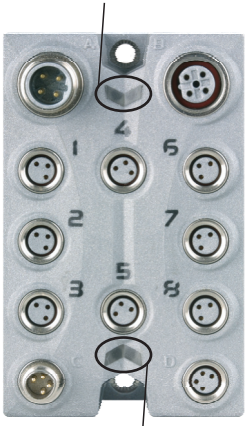
<table>
<tr><th>Figure</th><th>LED</th><th colspan="3">Description</th></tr>
<tr><td rowspan="15"><u>Status indicator 1:</u>
left: green; right: red
 
<u>Status indicator 2:</u>
left: green; right: red</td><td rowspan="5">Status indicator 1</td><td colspan="3">Status indicator - X2X Link.</td></tr>
<tr><td>Green</td><td>Red</td><td>Description</td></tr>
<tr><td>Off</td><td>Off</td><td>No supply via X2X Link</td></tr>
<tr><td>On</td><td>Off</td><td>X2X Link supplied, communication is functioning</td></tr>
<tr><td>Off</td><td>On</td><td>X2X supplied, but X2X communication is not functioning</td></tr>
<tr><td>On</td><td>On</td><td>Preoperational: X2X Link supplied, module not initialized</td></tr>
<tr><td>1 - 8</td><td colspan="3">Input / output status of the corresponding channel. The LEDs are orange.</td></tr>
<tr><td rowspan="9">Status indicator 2</td><td colspan="3">Status indicator for module function.</td></tr>
<tr><td>LED</td><td>Status</td><td>Description</td></tr>
<tr><td rowspan="4">Green</td><td>Off</td><td>Module supply not connected</td></tr>
<tr><td>Single flash</td><td>Reset mode</td></tr>
<tr><td>Blinking</td><td>Preoperational mode</td></tr>
<tr><td>On</td><td>RUN mode</td></tr>
<tr><td rowspan="4">Red</td><td>Off</td><td>Module supply not connected or everything is OK</td></tr>
<tr><td>On</td><td>Error or reset state</td></tr>
<tr><td>Single flash</td><td>Warning/error for an I/O channel. Level monitoring for digital outputs has been triggered.</td></tr>
<tr><td>Double flash</td><td>Supply voltage not in the valid range</td></tr>
</table>

Table 175: DM1321 - Status LEDs

6.2.6 Connection elements

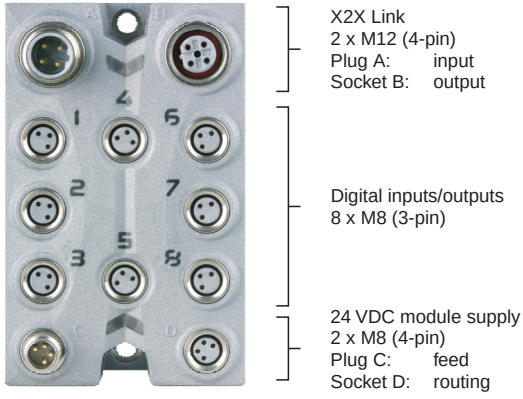


Figure 89: DM1321 - Connection elements

6.2.7 X2X Link

The DM1321 module is connected to the X2X Link with pre-assembled cables. The connection is made using a circular plug (2 x M12, 4-pin).

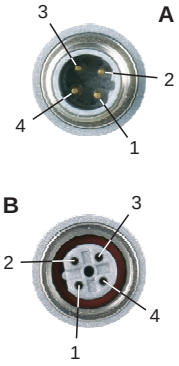
Connection	Pin assignments	
	**Pin**	**Name**
	1	X2X+
	2	X2X
	3	X2X⊥
	4	X2X\
	A ... B-coded plug in the module, input B ... B-coded socket in the module, output SHLD ... Shield connection made via threaded insert in the module	

Table 176: DM1321 - X2X Link

6.2.8 Digital inputs/outputs

The digital inputs/outputs are connected using circular plugs (8 x M8, 3-pin).

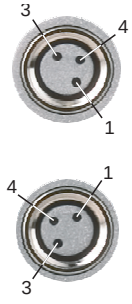
Connection	Pin assignments	
	**Pin**	**Name**
	1	24 VDC sensor/actuator supply [1]
	3	GND
	4	Input / Output x
	1) Sensors/actuators should not be supplied externally.	

Table 177: DM1321 - Digital inputs/outputs

6.2.9 24 VDC module supply

The module supply connection is made using circular plugs (2 x M8, 4-pin). The supply feed is connected via plug C. Socket D is used for routing the supply to other modules.

The maximum permitted current for the circular plug is 8 A.

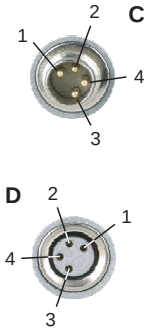
<table>
<tr><th>Connection</th><th colspan="2">Pin assignments</th></tr>
<tr><td rowspan="6"> 
</td><th>Pin</th><th>Name</th></tr>
<tr><td>1</td><td>24 VDC</td></tr>
<tr><td>2</td><td>24 VDC</td></tr>
<tr><td>3</td><td>GND</td></tr>
<tr><td>4</td><td>GND</td></tr>
<tr><td colspan="2">C ... Plug on the module, supply feed
D ... Socket on the module, supply routing</td></tr>
</table>

Table 178: DM1321 - 24 VDC module supply

6.2.10 Input/output circuit diagram

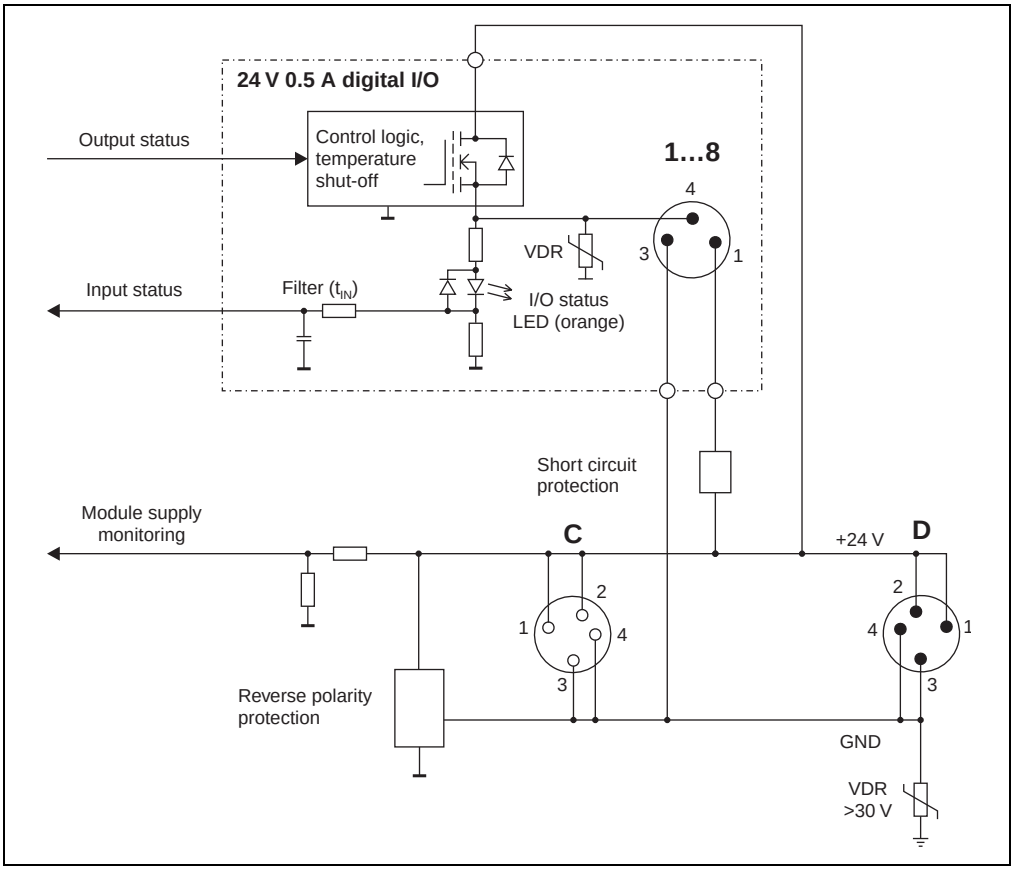


Figure 90: DM1321 - Input/output circuit diagram

6.2.11 Monitoring the module supply

The supply voltage for the inputs-/outputs is monitored. The status and the current voltage value can be read.

6.2.12 Output monitoring

The output states are compared to the set values on the module. The control for the output driver is used for the set states. The status of each individual channel can be read.

6.2.13 Switching inductive loads

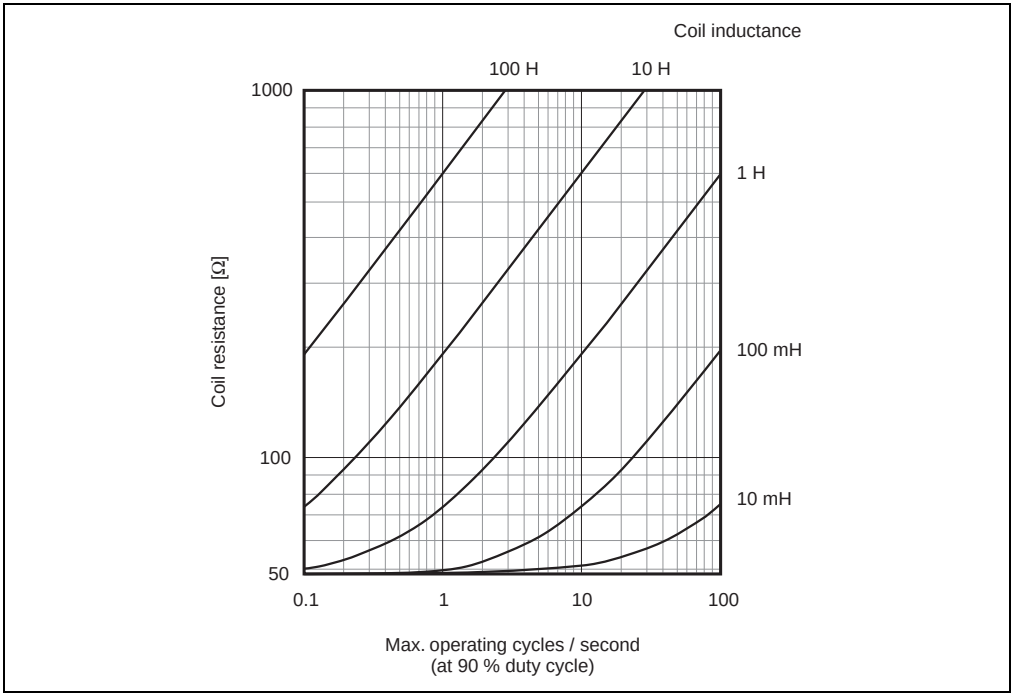


Figure 91: DM1321 - Switching inductive loads

6.2.14 Module addressing

Modules are addressed automatically. No settings are required on the module.

6.2.15 Register

The registers are divided in cyclic and acyclic registers.

Register type	Register ID
Cyclic	Bank 0
Acyclic	Bank 32

Table 179: DM1321 - Register ID

The following table contains the registers supported by the module:

Register	Description	Configuration					
		Data type	Length	Read	Write	Cyclic	Acyclic
Bank 0							
0	Digital inputs 1 - 8	USINT	1	●		●	●
2	Digital outputs 1 - 8	USINT	1		●	●	●
4	Event counter 1	UINT	1	●		●	●
6	Event counter 2	UINT	1	●		●	●
16	I/O mask	USINT	1		●	●	●
18	Input filter	USINT	1		●	●	●
20	Configuration counter channel 1	USINT	1		●	●	●
22	Configuration counter channel 2	USINT	1		●	●	●
26	Positive edge input latch (starting version V1.20)	USINT	1	●		●	●
28	Acknowledge input latch (starting version V1.20)	USINT	1	●	●	●	●
30	Status of the outputs	USINT	1	●		●	●
Bank 32							
0	B&R ID code	UINT	1	●			●
4	Status - Operating limits	USINT	1	●			●
16	Current module supply voltage	USINT	1	●			●

Table 180: DM1321 - Register overview

6.2.16 Cyclic register (bank 0)

Digital inputs

Unfiltered

The input status is registered with a fixed offset with respect to the network cycle and is transferred in the same cycle.

Filtered

The filtered status is registered with a fixed offset with respect to the network cycle and is transferred in the same cycle. Filtering takes place asynchronous to the network in a 200 µs grid with a network-related jitter of up to 50 µs.

Digital outputs

The output status is transferred to the output channels using a fixed offset to the network cycle.

Event counter

Depending on the mode, contains the count value or the gate time of channel 1 and channel 2.

I/O mask

Defines channel handling using output monitoring or filtering. Outputs are monitored but not filtered.

Bit	Description
0	0 ... Channel 1 is configured as an input 1 ... Channel 1 is configured as an output
1	0 ... Channel 2 is configured as input 1 ... Channel 2 is configured as an output
2	0 ... Channel 3 is configured as an input 1 ... Channel 3 is configured as an output
3	0 ... Channel 4 is configured as input 1 ... Channel 4 is configured as an output
4	0 ... Channel 5 is configured as an input 1 ... Channel 5 is configured as an output
5	0 ... Channel 6 is configured as input 1 ... Channel 6 is configured as an output
6	0 ... Channel 7 is configured as an input 1 ... Channel 7 is configured as an output
7	0 ... Channel 8 is configured as input 1 ... Channel 8 is configured as an output

Input filter

Filtering for all digital inputs can be configured using this register.

Value	Filter
0	No SW filter
2	0.2 ms
4	0.4 ms
:	:
250	25 ms - higher values are limited to this value

Table 181: DM1321 - Input filter

Configuration of counter channels 1 and 2

Bit	Description
0 - 2	000 ... Counter frequency= 48 MHz (only with gate measurement) 001 ... Counter frequency= 3 MHz (only with gate measurement) 010 ... Counter frequency= 187.5 kHz (only with gate measurement)
3 - 4	0
5	0 ... No influence on the counter 1 ... Delete counter
6 - 7	00 ... Event counter measurement 01 ... Gate measurement

Event counter operation

The falling edges are registered on the counter input.

The counter status is registered with a fixed offset with respect to the network cycle and is transferred in the same cycle.

Gate measurement

Information:

Only one of the counter channels at a time can be used for gate measurement.

The time of rising to falling edges for the gate input is registered using an internal frequency. The result is checked for overflow ($FFFF).

The recovery time between measurements must be >100 µs.

The measurement result is transferred with the falling edge to the result memory.

Positive edge input latch

This register is included in Firmware version V 1.20 and higher.

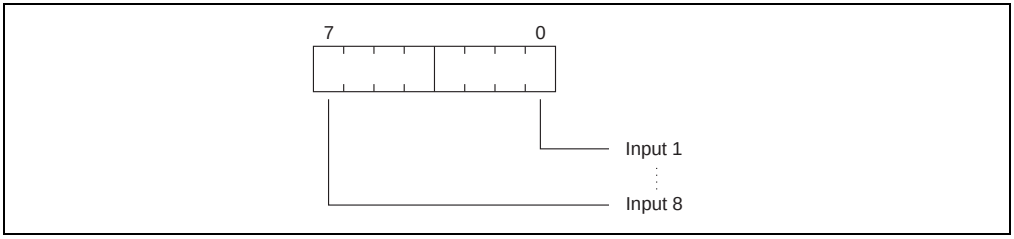
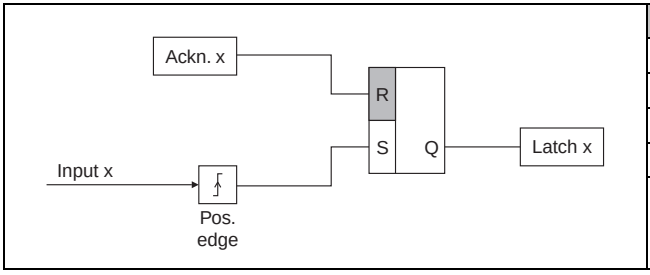


Figure 92: DM1321 - "Positive edge input latch" register

Using this register, the positive edges of the input signal can be latched with a resolution of 200 µs. With the register "acknowledge input latch", the input latch is either reset or prevented from latching.

It works in the same way as a dominant reset RS flip-flop.



R	S	Q	Status
0	0	x	Do not change
0	1	1	Set
1	0	0	Reset
1	1	0	Reset

Table 182: DM1321 - "Positive edge input latch" register, the function principle

Input latch acknowledgement

This register is included in Firmware version V 1.20 and higher.

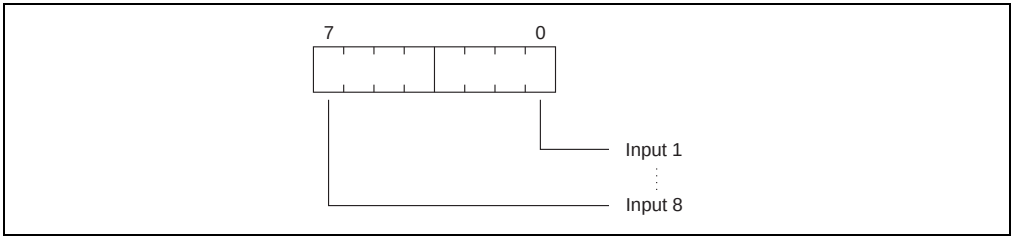


Figure 93: DM1321 - "Acknowledge input latch" register

With the register "Acknowledge input latch", the input latch is reset channel by channel.

Status of the outputs

On the module, the output states (for the outputs defined in the output mask) are compared with the set states. The control for the output driver is used for the set states.

A change in the output status resets the monitoring for this output. The status of each individual channel can be read. A change in the monitoring status generates an error message.

Bit	Description
0	0 ... Channel 1: No error 1 ... Channel 1: Short circuit or overload
1	0 ... Channel 2: No error 1 ... Channel 2: Short circuit or overload
2	0 ... Channel 3: No error 1 ... Channel 3: Short circuit or overload
3	0 ... Channel 4: No error 1 ... Channel 4: Short circuit or overload
4	0 ... Channel 5: No error 1 ... Channel 5: Short circuit or overload
5	0 ... Channel 6: No error 1 ... Channel 6: Short circuit or overload
6	0 ... Channel 7: No error 1 ... Channel 7: Short circuit or overload
7	0 ... Channel 8: No error 1 ... Channel 8: Short circuit or overload

6.2.17 Acyclic register (bank 32)

B&R ID code

Code for module identification ($1311).

Status register operating limits

Bit	Description
0	0 ... Module supply within the warning limits (18 - 30 V) 1 ... Module supply outside the warning limits (<18 V or >30 V)
1 - 7	0

Current module supply voltage

The supply voltage of the module is measured. Resolution: 1 V

6.2.18 Function models

A function model describes the registers for the module (memory model) which are available for the application. Only these registers are processed on the module during each cycle and cyclically transferred using the bus. The cycle time can be minimized by selecting the correct function model.

Minimum cycle time

The minimum cycle time is the minimum time needed for the bus cycle to be shut down without a communication error or malfunction occurring. It should be noted that very fast cycles reduce the idle time needed for handling monitoring, diagnostics and acyclic commands.

Minimum I/O update time

The minimum I/O update time refers to the minimum time it takes for the bus cycle to shut down, so that in each cycle an I/O update takes place.

Digital module - Function model (default)

Function model 0					
Register	Description	Configuration			
		Data type	Length	Read	Write
0	Digital inputs	USINT	1	●	
2	Digital outputs	USINT	1		●
16	I/O mask	USINT	1		●
18	Input filter	USINT	1		●
30	Status of the outputs	USINT	1	●	

Table 183: DM1321 - Function model 0 (digital module)

Minimum cycle time	
Without filtering	150 µs
With filtering	200 µs

Table 184: DM1321 - Minimum cycle time for function model 0

Minimum I/O update time	
Without filtering	150 µs
With filtering	200 µs

Table 185: DM1321 - Minimum I/O update time for function model 0

Function model - Digital module (with input latch)

Function model 2					
Register	Description	Configuration			
		Data type	Length	Read	Write
0	Digital inputs	USINT	1	●	
2	Digital outputs	USINT	1		●
16	I/O mask	USINT	1		●
18	Input filter	USINT	1		●
26	Positive edge input latch (starting version V1.20)	USINT	1	●	
28	Acknowledge input latch (starting version V1.20)	USINT	1	●	●
30	Status of the outputs	USINT	1	●	

Table 186: DM1321 - Function model 2 (digital module with input latch)

Minimum cycle time	
Without filtering	150 µs
With filtering	200 µs

Table 187: DM1321 - Minimum cycle time for function model 2

Minimum I/O update time	
Without filtering	150 µs
With filtering	200 µs

Table 188: DM1321 - Minimum I/O update time for function model 2

Function model - Digital and counter module

Function model 1					
Register	Description	Configuration			
		Data type	Length	Read	Write
0	Digital inputs	USINT	1	●	
2	Digital outputs	USINT	1		●
4	Event counter 1	UINT	1	●	
6	Event counter 2	UINT	1	●	
16	I/O mask	USINT	1		●
18	Input filter	USINT	1		●
20	Configuration counter channel 1	USINT	1		●
22	Configuration counter channel 2	USINT	1		●
26	Positive edge input latch (starting version V1.20)	USINT	1	●	
28	Acknowledge input latch (starting version V1.20)	USINT	1	●	●
30	Status of the outputs	USINT	1	●	

Table 189: DM1321 - Function model 1 (digital and counter module)

Minimum cycle time	
Counter operation	250 µs

Table 190: DM1321 - Minimum cycle time for function model 1

Minimum I/O update time	
Counter operation	250 µs

Table 191: DM1321 - Minimum I/O update time for function model 1